Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7- 21, 59-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243) and either one of Hunt et al. ("High Temperature Superconductor Josephson Weak Links") or Jia et al. (Effect of chemical and ion-beam…).

Figure 2 of Harada shows a Josephson junction having a crystalline substrate MgO, a YBCO electrode formed on and epitaxial to the substrate (page 1389, column 1, lines 4-7), an insulator a-YSZ, a barrier comprising a plasma-treated surface of the YBCO (page 1387, column 1, second paragraph), and a YBCO counter-electrode formed directly on and epitaxial to the barrier.

Chan teaches with respect to the cover figure to form insulator 48 epitaxially on YBCO 46 (column 6, lines 25-32).

It would have been obvious to form an epitaxial insulator on the Harada device instead of a-YSZ, in order to obtain the higher quality crystalline material obtained by epitaxial growth.

With respect to claims 2-4, a process limitation carries weight in a claim drawn to a product only when distinct structure is produced by the process. *In re Thorpe*, 227

USPQ 964 (Fed. Cir. 1985). There is no evidence of record to show that the process steps recited would necessarily give rise to a barrier layer distinct from that of Harada.

With respect to claim 5, both of the Harada YBCO layers have their c-axis perpendicular to the substrate (page 1389, column 1, lines 4-7). Therefor the top plane of the lower YBCO must be an a-b plane, and a junction is formed in that plane.

With respect to the layer in-between the superconducting layers wherein the barrier layer is produced by ion-milling the superconducting layer, Hunt teaches the claimed process limitations (pages 3 and 4).

Jia teach forming barrier layers by ion-etching a superconductor (pg 3635, Fig 2).

Therefore, it would have been obvious to one of ordinary skill in the art to provide a non-superconducting, ion modified surface layer of a superconducting oxide in Harada in order to provide a barrier layer between two superconducting oxides as taught by Hunt or Jia.

Harada et al. fail to teach the claimed I_cR_n product.

However, Hunt teach that it is known for YBCO with microbridges to exhibit an I_cR_n product of around 1.03 mV at a temperature of 4.2 K and an I_cR_n product of around 450 μV a temperature of 77 K (pg 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time applicant's invention was made to provide the claimed I_cR_n product in Harada because the fabrication method for making YBCO devices exhibiting the claimed I_cR_n product are known as taught by Hunt.

With respect to claims 63 and 64, it appears that the process of making the junctions is substantially similar to the claimed invention such that the properties of the junctions of the prior art are substantially similar to those of the claimed invention.

While it appears that neither Hunt nor Jia explicitly disclose a substantially uniform ion-milled barrier layer, it appears that Hunt suggests that the Hunt teaches ion-damage barrier chips fabricated using Ar ions to etch tapered YBCO edges (page 005). it appears that Hunt treats the YBCO edge in a uniform manner.

Jia also appear to teach a substantially uniform barrier layer (pg. 3635,3636).

Therefore, it would have been obvious to one of ordinary skill in the art at the time applicant's invention was made to provide a substantially uniform barrier in Harada et al. in order to provide a barrier layer between two superconducting oxides as taught by Hunt or Jia.

As to claims 65-74, it appears that Jia teaches a substantially similar process of making the barrier layer as that of the claimed invention such that the properties of the barrier layer of Jia are substantially similar to the properties of the barrier layer of the claimed invention.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243) and Laibowitz et al. ("All high T_c edge junctions and SQUIDS").

Laibowitz et al. teaches at the bottom of column 1 of page 686 that transport along the a-b plane direction has a longer coherence length and higher current density.

It would have been obvious to arrange a junction perpendicular to the a-b plane for these reasons. The device of Harada in figure 2 has a perpendicular portion of the junction that would be perpendicular to the a-b plane, because the c direction is perpendicular to the MgO substrate.

Claims 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243) and Laibowitz et al. ("All high T_c edge junctions and SQUIDS") and Satoh et al. ("Effect of Lanthanum Doping of YbaCuO…").

Harada et al. fail to teach the claimed I_cR_n product.

Satoh teach a method of making YBCO (pg 1) wherein lanthanum doped YBCO produces a higher I_cR_n product than that of pure YBCO (pp. 2, 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time applicant's invention was made to provide a higher I_cR_n product than that of pure YBCO in Harada et al. because it is known to dope YBCO with lanthanum in order to obtain high I_cR_n product.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize an I_cR_n product, since it has been held that discovering an optimum value or a result effective variable involved only routine skill in the art. In re Boesch, 617 F.2nd 272, 205 USPQ 215 (CCPA 1980). The artisan would have been motivated to optimize an I_cR_n product by the reasoning that higher I_cR_n product enables annealing at higher temperatures for longer durations as taught by Satoh.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL A. WARTALOWICZ whose telephone number is (571)272-5957. The examiner can normally be reached on 8:30-6 M-Th and 8:30-5 on Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stanley Silverman can be reached on (571) 272-1358. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Wartalowicz
September 21, 2008

/Steven Bos/
Primary Examiner
A.U. 1793